REMARKS

Claims 1-20 are pending in the application.

Claims 1, 5-6, 9, 12, 14-15, 17, and 19-20 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 5,883,534 to Kondoh et al. ("Kondoh"). Claims 2-4, 7-8, 10-11, 13, 16, and 18-19 are objected to.

In view of the amendments and remarks herein, Applicant respectfully traverses the rejections and asks that they be withdrawn.

Claims 2-8, 10-13, and 15-20

The office action indicated that claims 2-4, 7-8, 10-11, 13, 16, and 18-19 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant thanks the Patent Office for the indication of allowability.

Applicant has amended claims 2, 5-7, 10-12, and 15-20 so that claims 2-8, 10-13, and 15-20 have either been rewritten in independent form as suggested, or have been amended to depend from a claim rewritten in independent form.

For at least this reason, Applicant believes that claims 2-8, 10-13, and 15-20 are now in condition for allowance.

Claims 1, 9, and 14

Claims 1, 9, and 14 have been amended. Claim 1 is patentable over Kondoh at least because Kondoh neither teaches nor suggests "the input signal comprising a first clock signal and a second clock signal," as recited in claim 1. Claims 9 and 14 have been amended to include similar features.

Rather than comprising a first clock signal and a second clock signal, the input signal of Kondoh is a single clock signal (see, e.g., FIG. 26 of Kondoh). Since Kondoh does not teach or suggest this feature, claims 1, 9, and 14 are patentable over Kondoh.

Further, there is no motivation to modify Kondoh to include an input signal having first and second clock signals, since Kondo is directed to "a waveform shaping device for converting the duty ratio, the frequency and the like of a clock signal, and to a clock supply apparatus formed by combining a DLL device with the waveform shaping device." (See, e.g., column 1, lines 6-11 of Kondoh). That is, since Kondoh is directed to shaping the waveform of a particular clock signal, there is no motivation to provide an input signal having first and second clock signals.

For at least the above reasons, claims 1, 9, and 14 are patentable over Kondoh.

Attached is a marked-up version of the changes being made by the current amendment.

CONCLUSION

In view of the amendments and remarks herein, Applicant believes that claims 1-20 are in condition for allowance and asks that all claims be allowed. If the Examiner has any questions regarding this response, the Examiner is invited to call the undersigned at (858) 678-5070.

Enclosed is a $252.00 check for excess claim fees. Please apply any unpaid charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Version with markings to show changes made

In the claims:

Claims 1, 2, 5-7, 9-12, and 14-20 have been amended as follows:

1. (Amended) A device, comprising:

a delay lock loop circuit responsive to an input signal to delay the input signal by a first period and to generate an analog control signal having an amplitude; and

a delay circuit coupled to the delay lock loop circuit and responsive to the input signal, the delay circuit being responsive to the analog control signal from the delay lock loop circuit to delay the input signal by a second period as a function of the analog control signal amplitude, the input signal comprising a first clock signal and a second clock signal.

2. (Amended) [The device of claim 1,] A device, comprising:

a delay lock loop circuit responsive to an input signal to delay the input signal by a first period and to generate an analog control signal having an amplitude; and

a delay circuit coupled to the delay lock loop circuit and responsive to the input signal, the delay circuit being

responsive to the analog control signal from the delay lock loop circuit to delay the input signal by a second period as a function of the analog control signal amplitude, wherein the input signal comprises complimentary input clock signals.

5. (Amended) The device of claim [1] 2, wherein the delay lock loop circuit further comprises:

at least one delay cell; and

a phase detector responsive to the input signal and responsive to an output signal from the at least one delay cell to produce a control signal.

6. (Amended) The device of claim [1] 2, wherein the delay circuit further comprises at least one delay cell responsive to the control signal from the delay lock loop circuit.

7. (Amended) The device of claim [1] 2, further comprising;

a latch circuit having a first input to receive an input data signal and a second input to receive one of an output from the delay circuit and an output from the delay lock loop circuit.

9. (Amended) A device, comprising:

a delay lock loop circuit responsive to a first clock signal of an [first] input signal to delay the first [input signal] clock signal by a first period and to generate an analog control signal having an amplitude; and

a delay circuit coupled to the delay lock loop circuit and responsive to a second clock signal of the input signal, the delay circuit being responsive to the analog control signal from the delay lock loop circuit to delay the second clock signal by a second period as a function of the analog control signal amplitude.

10. (Amended) [The device of claim 9]A device, comprising:

a delay lock loop circuit responsive to a first input signal to delay the first input signal by a first period and to generate an analog control signal having an amplitude; and

a delay circuit coupled to the delay lock loop circuit and responsive to a second input signal, the delay circuit being responsive to the analog control signal from the delay lock loop circuit to delay the second signal by a second period as a function of the analog control signal amplitude, wherein the

first signal and the second signal comprise complimentary clock signals.

11. (Amended) The device of claim [9] 10 further comprising a latch circuit, the latch being responsive to one an output of the delay lock loop circuit and an output of the delay circuit.

12. (Amended) The device of claim [9] 10 wherein the delay lock loop circuit comprises at least one delay cell.

14. (Amended) A method, comprising:

receiving an input signal comprising a first clock signal and a second clock signal [first signal and a second signal];

using a delay lock loop circuit to delay the first clock signal by a first period;

controlling the first period as a function of an analog control signal having an amplitude; and

using a delay circuit to delay the second clock signal by a second period in response to the analog control signal amplitude from the delay lock loop circuit.

15. (Amended) The method of claim 1[4]6, wherein the using the delay lock loop circuit comprises configuring the delay lock loop circuit with at least one delay cell.

16. (Amended) [The method of claim 14 further comprising] A method, comprising:

receiving a first signal and a second signal;

using a delay lock loop circuit to delay the first signal by a first period;

controlling the first period as a function of an analog control signal having an amplitude;

using a delay circuit to delay the second signal by a second period in response to the analog control signal amplitude from the delay lock loop circuit; and

activating a latch circuit in response to at least one of an output from the delay lock loop circuit and an output from the delay circuit.

17. (Amended) The method of claim 1[4]6, wherein the receiving the first signal and the second signal further comprises receiving a first clock signal and a second clock signal.

18. (Amended) The method of claim 1[4]6, wherein the receiving the first signal and the second signal further comprises receiving a first clock signal and a second clock signal and the method further comprising activating a latch circuit on a rising edge of one of the first delayed clock signal and the second delayed clock signal.

19. (Amended) The method of claim 1[4]6, wherein the first period and the second period are substantially the same.

20. (Amended) The method of claim 1[4]6, wherein the using the delay circuit further comprises configuring the delay circuit with at least one delay cell and using the control signal to adjust the at least one delay cell.